Boosting multiple bit computation with Hybrid P3N-8T SRAM chips for Image Applications

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Abstract— **The increasing frequency of multiple bit processing (MBP) on SRAM memory devices is causing leakage power consumption and a greater need for error code corrections (ECCs) in multimedia applications. To address this issue, a split bit approach is suggested to minimize redundancy and enhance corrective coverage. The pseudo bit line (PBL) topology is introduced to reduce errors and improve power-energy consumption, speed, and battery life. This design is implemented in SRAM-based encoders for real-time encoders on nanotechnology, enhancing power-energy consumption, speed, and battery life. The PBL-based PMOS-PMOS-NMOS (P3N) technique on static memory cells grants 1.92pW reduced power margins, faster transition speed, and reduced errors. Process simulations show enhanced leakage consumption of 55.439fW. The 2-bit truncated matrix is automatically and effectively generated, expressing its error detection and/or estimation capabilities. The proposed scheme's delay overhead is 10.15%, 13.26%, 21.2%, 4.5%, and 23.45% lower than existing Hamming, CMC, ECC for 5-bit adjacent error, eMRSC, and DICE-7-bit ECC techniques.**

Index Terms—**Energy efficiency, Leakage power, Low power design, Read operation, Static noise margin**

I. Introduction

Energy-efficient designs have become mere perceivable throughout years pondering on novel electronic gadgets. Recent designs consisting of System on Chip (SOCs) mainly exhibits enhanced performance with scaling transistor strength on minimal technology nodes. This perusal has resulted for stability and design complexities. Other techniques degrade the SRAM performance by minimalizing the access transistor sizes making them weaker, boosting/clamping the sensed Bit-Line (BL) voltage swing [12], or pseudo-charging with read-decoupled SRAM bit-cell designs [8] resulting in the increased layout structure. This concern was also noted in previous 8T/9T SRAM designs [5-11] due to large number of NMOS transistors which compels in slower processing in higher resolute based peripheral circuits like analog-to-digital converter (ADC) and digital-to-analog converter (DAC) [4]. Additionally, with the introduction of Carbon Nano-Tube Field-Effect Transistor (CNTFET) and Fin Field-Effect Transistor (FINFET) technology based designs, many complexities have been resolved enhancing the leakage current and PDP factor. Concurrently, these complex designs cost higher dynamic power and area consumption due to rigorous scaling [5]. This led to increased sensitivity and reliability during process variations [1]. CMOS technology based conventional SRAM memory cells have shown degraded data quality when transitioning between multiple rows/columns on lowest possible voltage due to pre-charged BL injecting errors during "0" bit node storage. This affects the stocking or leaking of unwanted data during read operation causing heating or swelling of batteries [3]. Moreover, it slows down the charging and discharging of BL owing up to 70% dissipation of active power and timing circuitry of the entire SRAM cell [5]. Thus, there is a need to enlighten a more stable scheme with higher efficiency, reliability and sensitivity. Diverse energy efficient SRAM designs majorly focusing on PDP reduction during read operation have shown encouraging results via various techniques like Adaptive BL transformations [3], Bit Sharing [4], Single-ended architectures [1, 5, 6], Voltage stacking [7], WL boosting [8], Bit-wise operations [9-11], Data searching etc. In contrast to this, we observed that schemes like Transient-Voltage-Collapsing (TVC), Word Line Over Drive (WLOD) [4], Word Line Under Drive (WLUD) [12] etc. have achieved their motive on higher frequency parameters and write noise margins conveniently. Summarizing the concerns during multiprocessing, we concluded that existing SRAM requires attention on various levels during designing to have balanced computations and data handling on multiple lower level applications.

This brief presents energy-efficient 6T-SRAM cell designs with PBL and PMOS-PMOS-NMOS topologies for real-time applications. It explores balanced SRAM structures for data computations and introduces techniques for reliable designs with a minimal supply of 0.25VDD under process variations. Techniques include a boosted PBL design array with improved read-write assist, a PMOS-PMOS-NMOS scheme for balancing multiple data access, and an improved SRAM design based on PBL and PMOS-PMOS-NMOS (P3N) design. Section III lists efficient schemes for balancing SRAM in mobile applications.

II. Proposed Ultra low SRAM Methodology

A. Activated WL based PBL Design Array

Fig.1 (a) displays the pseudo-in the WL scheme for shared PBL utilization leading to boosting of data transitions during multiprocessing overcoming sizing of transistors conflicts. Rigorous scaling weakens the design and efficiency during read-write accesses unbalancing row/column transitions. Selection of bits on rows/columns level to achieve the multiprocessing in timely

manner have affected the structures which is broadly discussed in section IV. Also, parasitic capacitance in BLB heats up system allowing '1' storage bit data even on low supply results in worse-case scenarios. This concern has challenged the dynamic power consumption and sensitivity of the architecture. To overcome this, sense amplifier based schemes has been considered for lowering the NBL and Drain-Induced Barrier Lowering (DIBL) related issues [4, 8] in CMOS technology. During write assist, the row based BLB and column based activated WL select a cell, which does not affect the stability during data selection. However, data selection based bit operations also leads to timing circuitry issues in 10T and 8T SRAMs [6-8]. Techniques foresaid mainly consumes mere energy-area consumption during PVT processes. Thus, the activation in programmed WL technique (see fig.1 (a)) achieves better outcomes in read/write structure disabling the BL swinging on lower scale or sub threshold domain based process variations boosting up the data which has been considered in this work.

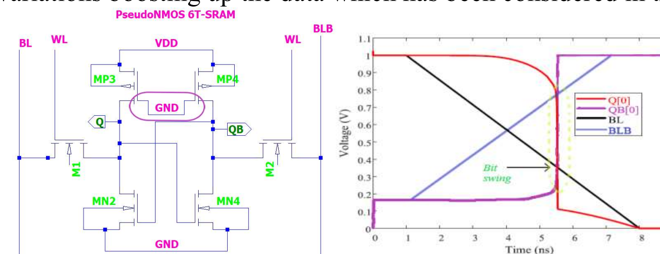


Fig.1. (a) PBL Schematic with WL activation and (b) Simulated Output displaying Bit swing in storage nodes.

B. Leakage control with PMOS-PMOS-NMOS technique

Bit swing causes data leakage in read access columns during off-stage or near threshold stages. Active sense amplifiers can leak '0' storage bit cells with minimal or maximum leakage, and idle cells in near threshold or off-stage areas are more susceptible to Process Voltage Temperature (PVT) conditions. This leads to reduced access in small transistors, limiting read access current and increasing the Signal-to-Noise (SNM) margin ratio. This imbalanced access pattern contributes to short circuits and total leakage current dissipation in access transistors. Various ultra-low voltage techniques have been implemented to enhance resilience, but still face leakage concerns. Novel designs have worked for quality metrics of SRAM design but face leakage current on BLB transistors with area coverage overhead. Processed worse-case scenarios during PVT variations display poor read/write operations and higher temperature, slowing down timing circuitry. Despite various hindering techniques and extra hardware, layout error-correction overhead becomes harder to fix. Adding two pull-up transistors could overcome most issues by improving low power transitions on sub threshold domains and maintaining leakage current dissipation. Activated WL in low supply domains can increase layout speed and avoid leakage. Hence, pseudo-charging of data bits will enhance further writing computations.

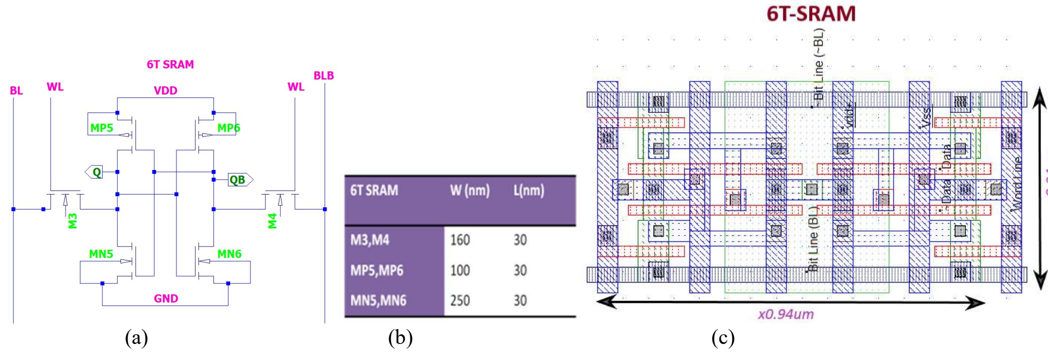
B. Proposed PMOS-PMOS-NMOS based Pseudo-NMOS (P3N) Ideology

The activated WL technique-based PBL (Positional Boltzmann) method is a novel approach to read disturbance reduction in Static memory, enabling aggressive voltage scaling. However, it faces leakage issues during read operation due to larger power consumption than targeted in scaled transistors. This is because the column-based NMOS footer is controlled by the column (BL) and the read path is controlled by the storage node (Q). This can affect the minimal flipping or swinging of pre-charged bits in the PBL pattern, leading to a leakage conflict. To address this issue, pseudo-differential and single-ended design schemes have been proposed, which consider the sense amplifier for better speed analysis. However, this approach lacks sensing stability due to device variability during process variations and parametric variations. The domino sensing scheme for parasitic capacitances in BL leads to data loss and inefficiency in power and energy. The proposed WL activated technique-based PBL structure with additional pull-up PMOSs is proposed to hold or isolate read bits by separating the activated WL from the charged up storage node (Q) during read disturbance. This allows for faster write operation in the BL while enabling bits in the BLB for read operation only. The P3N design focuses on feedback concerns during read operation, avoiding short-circuiting or data swinging/flipping caused by activated WL.

III. Design Overview

Fig.2 illustrates the conventional SRAM design dealing with multiple overheads like read-write stability, leakage current, density, design complexity, transistor size leading to area concerns. This has always made SRAM vulnerable to the process variations questioning its reliability towards various aspects (as discussed in previous section). In the proposed work, we employ an identical 6T SRAM bit cell to enhance its power efficiency during multiple data processing real-time applications. Also, Fig. 1 depicts our design supplying 250mV- 500mV voltage on 27°C room temperature at 20MHz on 32nm, 22nm and 16nm based CMOS technology. As discussed, due to frequent access, this cell faces large power consumption, read disturbances and stability margins which are explained thoroughly in further section on the spice simulations 1kb memory (32*32) array. Moreover, we chose 16nm as minimal node instead of 7nm due to greater power consumption in the design with the specified transistor size by 34.279nW. This needed improvement in its transistor sizes that could manage the greater area of circuit with design complexity which was another task to perform in future designs. Hence, to verify the reliability on 16nm CMOS technology for lower power

consumption, we run 2000 point Monte-Carlo (MC) simulation across PVT variations having mismatch of ±10% variations in minimal V_{DD}. Further, we primarily focus on the architectural parameters like – power, noise margins, PDP, leakage dissipation, area etc. which could be considered for optimization in further Section III followed by implementation based discussion indicating the dominant nature of power consumption in SRAM and how it can be handled extensively in Section IV.



6T SRAM	W (nm)	L(nm)
M3,M4	160	30
MP5,MP6	100	30
MN5,MN6	250	30

Fig.2. (a) Schematic, (b) transistor sizes and (c) layout of 6T SRAM

A. Read operation concern disturbing 6T SRAM computing

Throughout the years, severe transistor scaling has resulted in reduced performance during process fluctuations with power-delay trade-offs. In 6T SRAM, the transistor sizing for read operation issue during storage of "0" bit data input, an additional path was created in the 8T SRAM construction, causing power and area difficulties [6]. Figure 2 depicts a typical circuit diagram with transistor sizes and a CMOS design rules-based architecture (c). The rate of change in the BL is estimated for greater computing using (1), in which the voltage stabilizes the satisfactory proportions of current passing through bit-cell (ICELL), offering load capacitance (CBIT) of about 1fF to the BL for read-write margin, granting the circuit's power performance [2].

$$\frac{dV}{dt} = \frac{I_{Cell}}{C_{Bit}} \quad (1)$$

At the pre-charge to VDD in pre-read operation, the cell may be able to read the storage node as '1' at the cut off stage due to the parasitic capacitance (CPC) charging the BL, which may discharge the accessible capacitor in the form of leakage current (IL0). This discharge current in the real read scenario in CBIT swinging represented as (IL1) from VDD to VREF when reading the bit from 0 to 1 results in a delay expressed as,

$$\text{Reading } 0 = C_{\text{BIT}} = \frac{\text{V}_{\text{DD}} - \text{V}_{\text{REF}}}{I_{L0} + I_{L1}} \quad (2)$$

$$\text{Reading } 1 = C_{\text{BIT}} = \frac{\text{V}_{\text{DD}} - \text{V}_{\text{REF}}}{I_{L1}} \quad (3)$$

Therefore, the sensitivity pattern in BL during the discharging time in read operation in activated rows/columns will be:

Max (time in reading 0) < time (reading C_{PC} charged BL) < Min (time in reading 1) (4)

Earlier no process variations has been performed in 6T SRAM hence, threshold voltage (V_{TH}) in I_{CELL} is stored in M4 while the M3 stays in off staged mode with greater resistance and only gets activated when data "1" node is stored . Therefore, the drain current (I_{DS}) and the current below in sub-threshold domain (I_{GS}) will be expressed as

$$I_{DS} = I_{L1} e^{\frac{V_{GS} - V_{TH}}{n v_t}} e^{\frac{\lambda V_{DS}}{n v_t}} \left(1 - e^{\frac{-V_{DS}}{v_t}}\right) \quad (5)$$

Where, the sub-threshold voltages are affected on ground-to-source and drain-to-source level exponentially, as V_{GS} and V_{DS} having channel length (λ) having dimensionless number *n*. Therefore, total power overload (P_{TOTAL}) in SRAM processing takes place in the form of (6) were it represents as the sum of read (P_R)-write (P_W)-leakage (P_L) consumption.

$$P_{TOTAL} = P_W + P_R + P_L \quad (6)$$

III. Implementation

The study presents an innovative approach for an energy-efficient and variable resilient SRAM (P3N) cell. A 32*32 memory array and peripheral circuitry were designed and constructed in a 1kb configuration. The memory array operates according to the technique's design and development. The study examined power, current, delay time, and stability, as well as the tolerance of the cell on persistent word-line. Monte Carlo analysis was performed on all cells using 2000 samples to gain insight into accessed bit line patterns and ±10% variability. The study also investigated the reading-writing of the efficient PBL cell in activated WL mode with identical access transistor sizes. Technical/Electrical Quality Measures (EQM) revealed that the suggested SRAM cells performed well collectively compared to existing studies..

A. Proposed PPN based PBL technique

The study combines MP7 to MP10 PMOS transistors with an activated WL-based PBL architecture in fig. 3 for lower consumption and faster access. The new structure, similar to standard PBL behavior, adds 2 PMOS transistors to enhance the 'ON' stage pull-up behavior during data storage, enhancing BL performance with load capacitance during transitions. The design

layout takes 6.59% more area than the active PBL 6T structure. Simulations show that the storage nodes hold computation, with read almost equating to hold NM. The pseudo-effect enhances write ability, and the speed of write computation could offer greater transition production with lower consumption, but bit swinging due to activated WL in the circuit affects this..

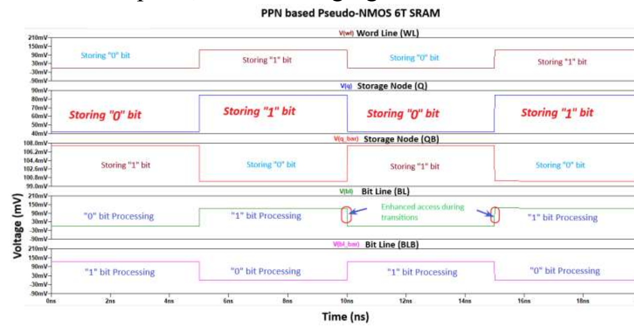


Fig. 3. PPN based Pseudo-NMOS 6T SRAM's simulation outputs displaying enhanced access during activation.

IV. Measurement Results

A. Performance parameters

The study focuses on read-write assist concerns in SRAM architectures, highlighting their timing circuitry sensitivity to process fluctuations, particularly in the sub-threshold area. The designs are tested with 250mV-500mV voltage at 27°C room temperature and 32*32 memory cell on 32nm, 22nm, and 16nm technology nodes. The activated WL-based SRAM cell layouts for area margin are evaluated using CMOS logic design rule. The EQM parameters are calculated based on the featured equations of all bit cells for comparison.

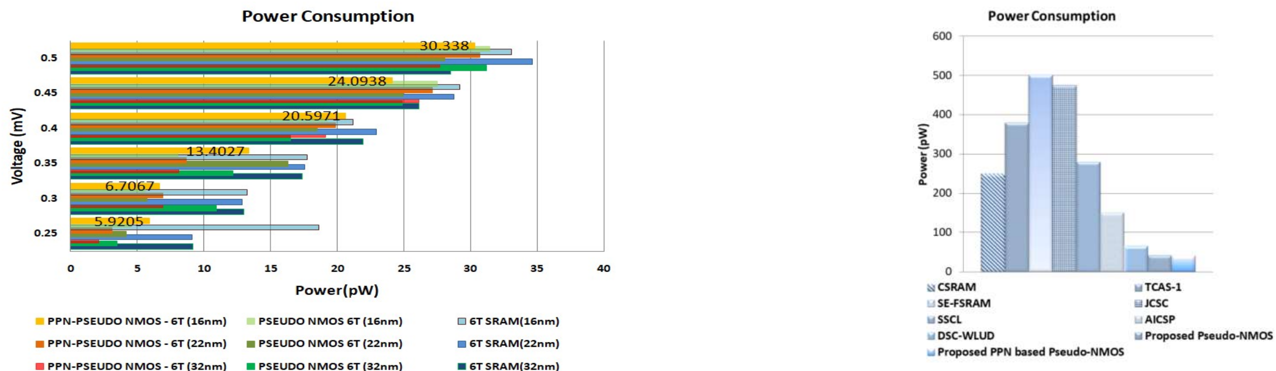


Fig.4. (a) Consumption of Power compared on SRAM designs supplying from 0.25-0.5 V_{DD} on 16nm, 22nm and 32nm nodes.(b) Comparing activated WL based Proposed PPN based PBL (P3N) SRAM cell with existing schematics

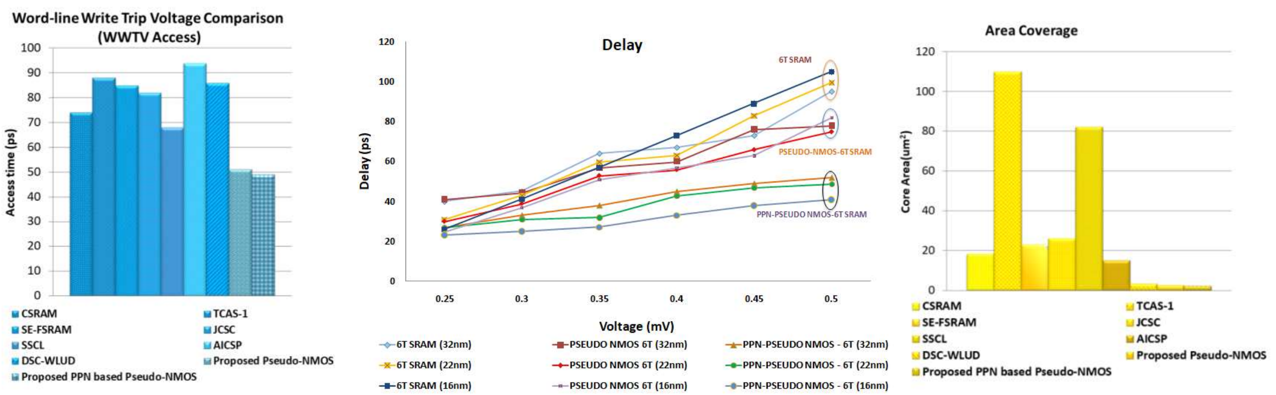


Fig. 5. (a) Consumption of WWTV access compared on SRAM designs supplying from 0.25-0.5 V_{DD}. (b) Delay compared on SRAM designs supplying from 0.25-0.5 V_{DD} on 16nm, 22nm and 32nm nodes.(b)read access (c) write access Consumption of Energy compared on SRAM designs supplying from 0.25-0.5 VDD on 16nm, 22nm and 32nm nodes.

1) **Power**
The study measured power-delay trade off during the read access of the bit line at the WL activation stage. The dynamic power, which includes source voltage and current during read-write computations, was analyzed. Various designs on 16nm,

22nm, and 32nm nodes were compared, showing minimal trade-offs. The consumption showed satisfactory results, but higher consumption was observed due to active power passage. Speed was increased at the expense of power-energy due to boosted activation in WL CSRAM design and pre-charging in selected 9T-SRAM cells. The Pseudo design provided 42% better consumption, while the P3N circuit showed an enhanced 88.9% performance due to double pull-up bit transitions during multiprocessing.

2) **Word-line Write Trip Voltage Comparisons**

Word-line Write Trip Voltage (WWTV) is the differential voltage that passes through the supply voltage VDD and the activated WL voltage at the crossed pull-up transistors. It quantifies the ease of writing into the SRAM. Single-ended architectures often fail to write the required bits during multiprocessing, and TCAS-1 faced read-write concerns due to partial selection of BL. Pseudocharging during BL reading disrupts the WWTV process during multi bit propagation, while SE-FRAM and JCSC face metal routing. Figure 5(a) compares estimated WWTV values of various present and proposed SRAMs. The dwindling of '1' storage node in AICSP results in bad WWTV. The proposed PPN-based design has greater WWTV and lower robustness in feedback path. The DSV-WLUD scheme enhances write margin due to row selective nature, but for a limited time.

TABLE I
PARAMETRIC VALUES BASED COMPARISON IN PROPOSED SRAM DESIGNS WITH EXISTING STUDIES

Year	**DSC-WLUD 2023 [1]**	**SE-FSRAM 2021[5]**	**JCSC 2019[6]**	**SSCL 2020[7]**	**TCAS-1 2017 [8]**	**AICSP 2021[9]**	**CSRAM 2021 [14]**	**WL activated Pseudo-NMOS**	**P3N (PPN based Pseudo-NMOS)**
CMOS TECHN(nm)	28	16	28	40	65	65	55	16	**16**
Cell	6T	6T	6T	8T	9T	6T	6T	6T	**6T**
Supply voltage(V)	0.9	0.8	0.8	0.6	0.35	0.4	1.2	0.25	**0.25**
Power consumption (pW)	N/A	N/A	8974.64	5279.20	N/A	N/A	N/A	6.554	**5.92**
Verification	Simulations	On-chip	On-chip	On-chip	On-chip	On-chip	Simulations	Simulations	Simulations
Read PDP (fJ)	436	2.69	444.5	N/A	N/A	N/A	N/A	**0.62**	0.94
Freq(MHz)	943	500	40	0.1	0.741	6	935	20	**20**
Energy access (pJ)	0.095	0.00219	0.0206	N/A	0.229	N/A	0.00325	0.0019	**0.0038**
Core Area(um^2)	0.338	23	26	82.1	110	15	1.83	**0.25**	1.1448
Leakage Power	N/A	N/A	9592mW	6859mW	N/A	N/A	N/A	92.74fW	**55.439fW**
FOM (fJ/V)	N/A	81.39	0.85	121.78	10.694	1.46	0.0089	0.000532	**0.000359**

3) **Delay**
The study focuses on the performance of a PBL 6T cell in read operation, focusing on the switching transition between bit storages. The results show that lower delay leads to faster access during transitioning, indicating enhanced circuit operation and greater computing access. However, switching concerns were noted in SE-FRAM and JSCS due to higher transistor sizes and bandwidth in the selected cells. The proposed P3N cell has the lowest read delay due to the pseudo-mechanism when the WL is turned ON, acquiring 10% of the supply during logic bit storage and 90% during the turned OFF stage of the initial input data. The performance loss in DSC-WLUD during PVT variations addresses higher BL leakage during multiprocessing due to lowered transistor current ratio, resulting in a failed sensing process. The multi-step WL control mechanism in AICSP improves read-write operation, requiring more sensitive timing circuitry during PVT variations. The DSC-WLUD scheme shows better timing circuitry using bit flipping but up to a certain range in selected rows during multi-processing. The study also highlights the transition delay in the FS corner when combined with the PBL design, allowing for better access to multiple bit transitions during PVT variations.

4) **Area**
The study focuses on the design of access transistors and their area requirements, addressing reliability issues in 9T SRAM and bit splitting in ZIG-ZAG SRAM. The proposed designs, activated WL-based Pseudo-NMOS and PPN-based layouts,

show improved contrast among bit cells by 9%, 10.9%, 7.15%, and 16.8% compared to trending designs. The BT effect enhances per pixel performance due to higher frequency, resulting in better coverage by 7.23% and 29.2%, respectively. The DSC-WLUD layout shows efficiency in area coverage but faces read disturbance issues, leading to unreliable behavior during multi-row activation schemes due to bit flipping. The results are presented in Fig. 5 (c).

5) **Figure of Merit (F.O.M.)**
This phenomenon confronts the parameters of SRAM architectures having trade-off performances [1]. Further, equation (9) employs the calculative amount consuming the energy per bit cell (E_{BIT}) tolerating the given nominal supply (V_{DD}). These terms depicts efficiency of the architectures. Here, Table I shows the estimated F.O.M. of the proposed designs in contrast to the existing ones which defines the remarkable read-write cell operations during multi bit processing.

$$F.O.M. = \frac{E_{BIT}}{V_{DD}} \quad (9)$$

Therefore, after calculating the F.O.M. of the existing and proposed circuit, the proposed designs showed encouraging results with better robustness, reliability and efficiency for the process variations as compared to the other architectures as we could figure out from the Table I. This analysis has been done for the first time as per our knowledge and is highly motivational for further operations. Concluding the novel designs showed encouraging results for balanced computations along with stability during multi data access.

V. Conclusion

Existing leakage power reduction techniques have affected SRAM chips at an exhaustive level which is affecting read-write operations during multi bit processing. Hence, various existing techniques have been analyzed featuring ECCs based PUFs and a hybrid topology has been introduced achieving greater computing making the design to work faster with enhanced read access and for longer duration. In this work, implementation of WL activated P3N based SRAM memory cell is designed. This technique is a hybrid of Pseudo Bit line (PBL) topology in PMOS-PMOS-NMOS (PPN) assembled architecture where both the activated PBL and PPN technologies are analyzed for 31.41pW leakage power efficiency during read-write operation displaying enhanced speed of 23 ps. Split WL activated PBL provided better performance in power consumption at minimal supply of 250mV of which is almost 85% better than the conventional designs. This analysis was done during feedback path attaining balanced multiple bit access which is highly motivating.

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